



US 20180301091A1

(19) **United States**(12) **Patent Application Publication**
Kuang et al.(10) **Pub. No.: US 2018/0301091 A1**(43) **Pub. Date: Oct. 18, 2018**(54) **OLED PIXEL DRIVING CIRCUIT AND
PIXEL DRIVING METHOD****Publication Classification**(71) Applicant: **SHENZHEN CHINA STAR
OPTOELECTRONICS
TECHNOLOGY CO., LTD.**, Shenzhen
City (CN)(51) **Int. Cl.**
G09G 3/3258 (2006.01)(52) **U.S. Cl.**
CPC ... **G09G 3/3258** (2013.01); **G09G 2320/0646**
(2013.01); **G09G 2320/0233** (2013.01); **G09G**
2320/045 (2013.01); **G09G 2300/0819**
(2013.01)(72) Inventors: **Jimu Kuang**, Shenzhen City (CN);
Yichien Wen, Shenzhen City (CN)(73) Assignee: **SHENZHEN CHINA STAR
OPTOELECTRONICS
TECHNOLOGY CO., LTD.**, Shenzhen
City (CN)(57) **ABSTRACT**

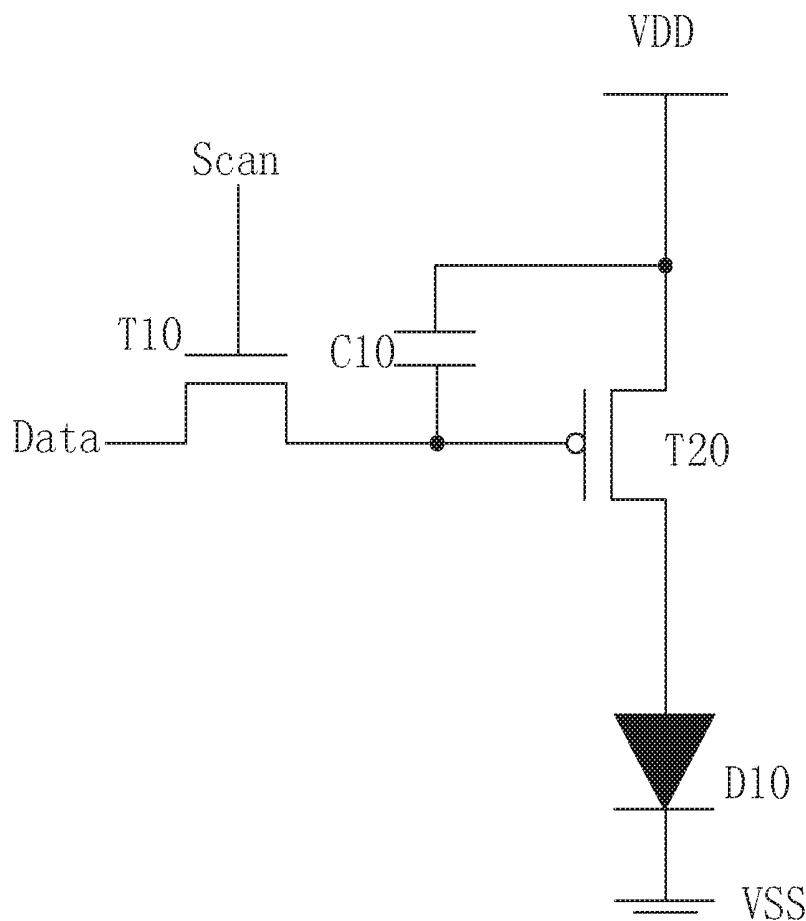
The present invention provides an OLED pixel driving circuit and a pixel driving method. The OLED pixel driving circuit utilizes the 7T2C structure, and comprises a first N type thin film transistor (T1), a second N type thin film transistor (T2), a third N type thin film transistor (T3), a fourth N type thin film transistor (T4), a fifth P type thin film transistor (T5), a sixth N type thin film transistor (T6), a seventh P type thin film transistor (T7), a first capacitor (C1), a second capacitor (C2) and an organic light emitting diode (D1), and the first scan signal (Scan1), the second scan signal (Scan2), the third scan signal (Scan3), the light emitting control signal (EM) and the data signal (Data) are combined with one another to correspond to a reset stage, a threshold voltage detection stage, a program stage and a light emitting stage one after another.

(21) Appl. No.: **15/519,840**(22) PCT Filed: **Mar. 16, 2017**(86) PCT No.: **PCT/CN2017/076862**

§ 371 (c)(1),

(2) Date: **Apr. 18, 2017**(30) **Foreign Application Priority Data**

Feb. 24, 2017 (CN) 201710104789.9



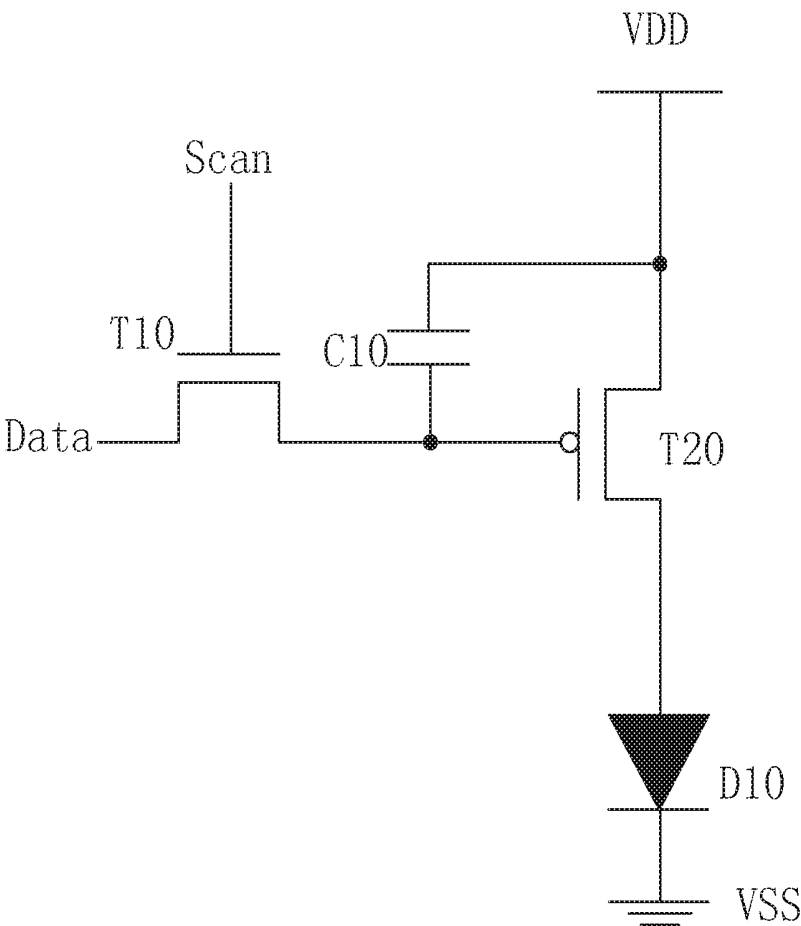


Fig. 1

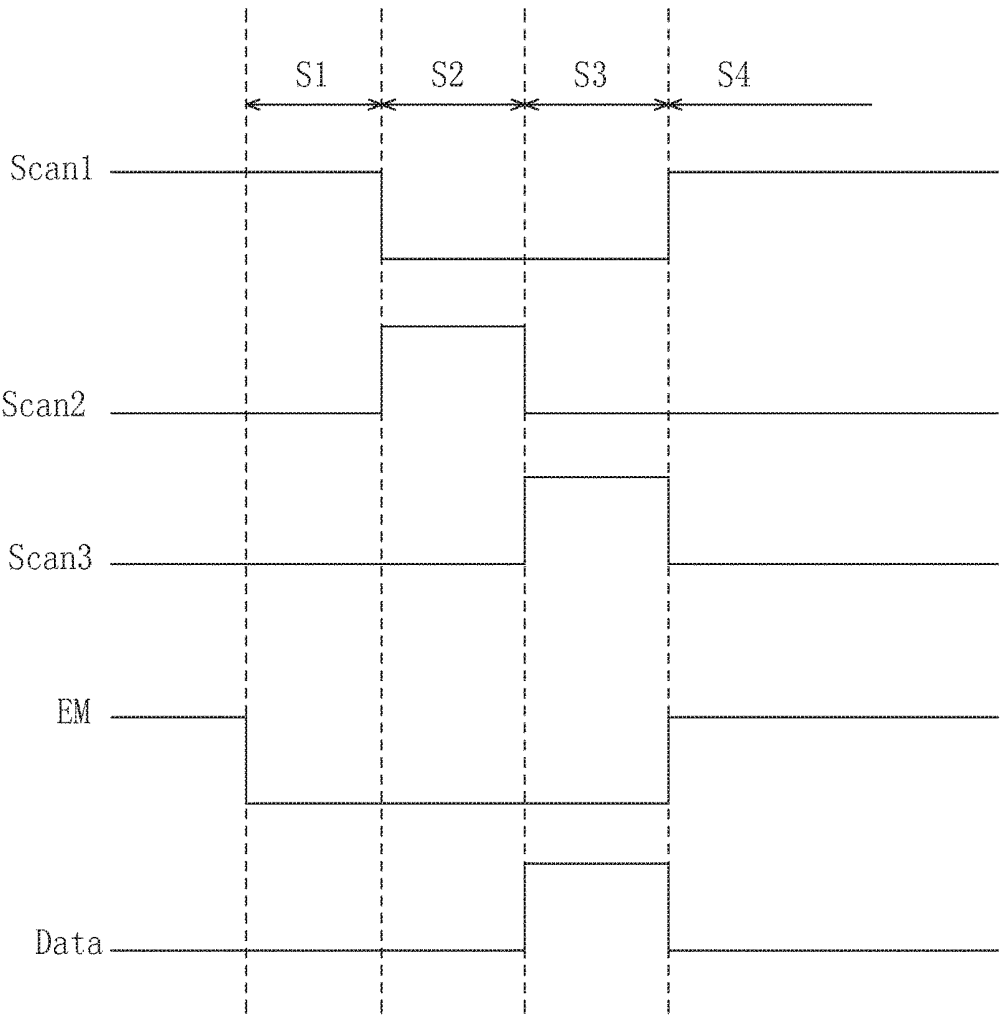


Fig. 3

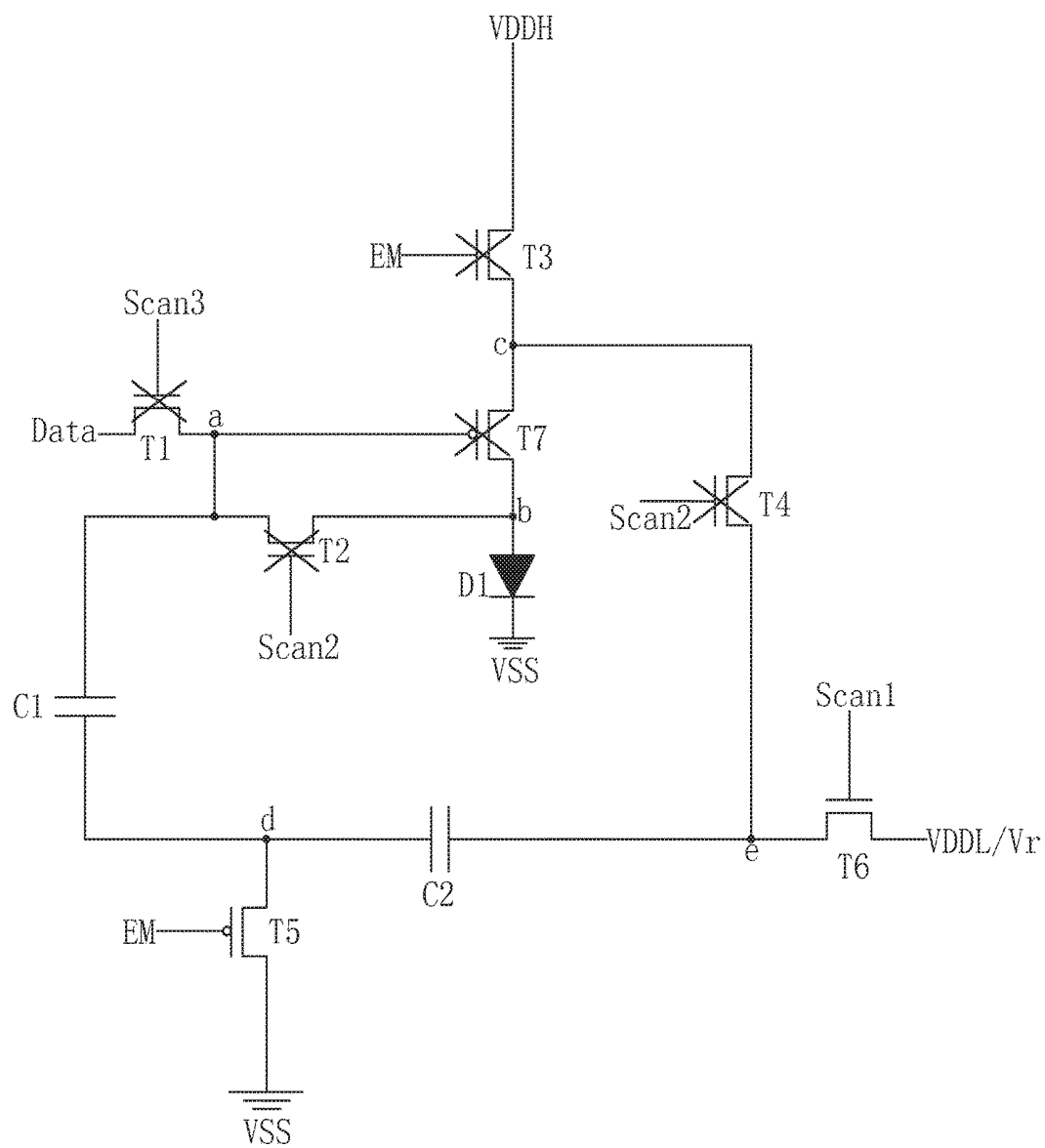


Fig. 4

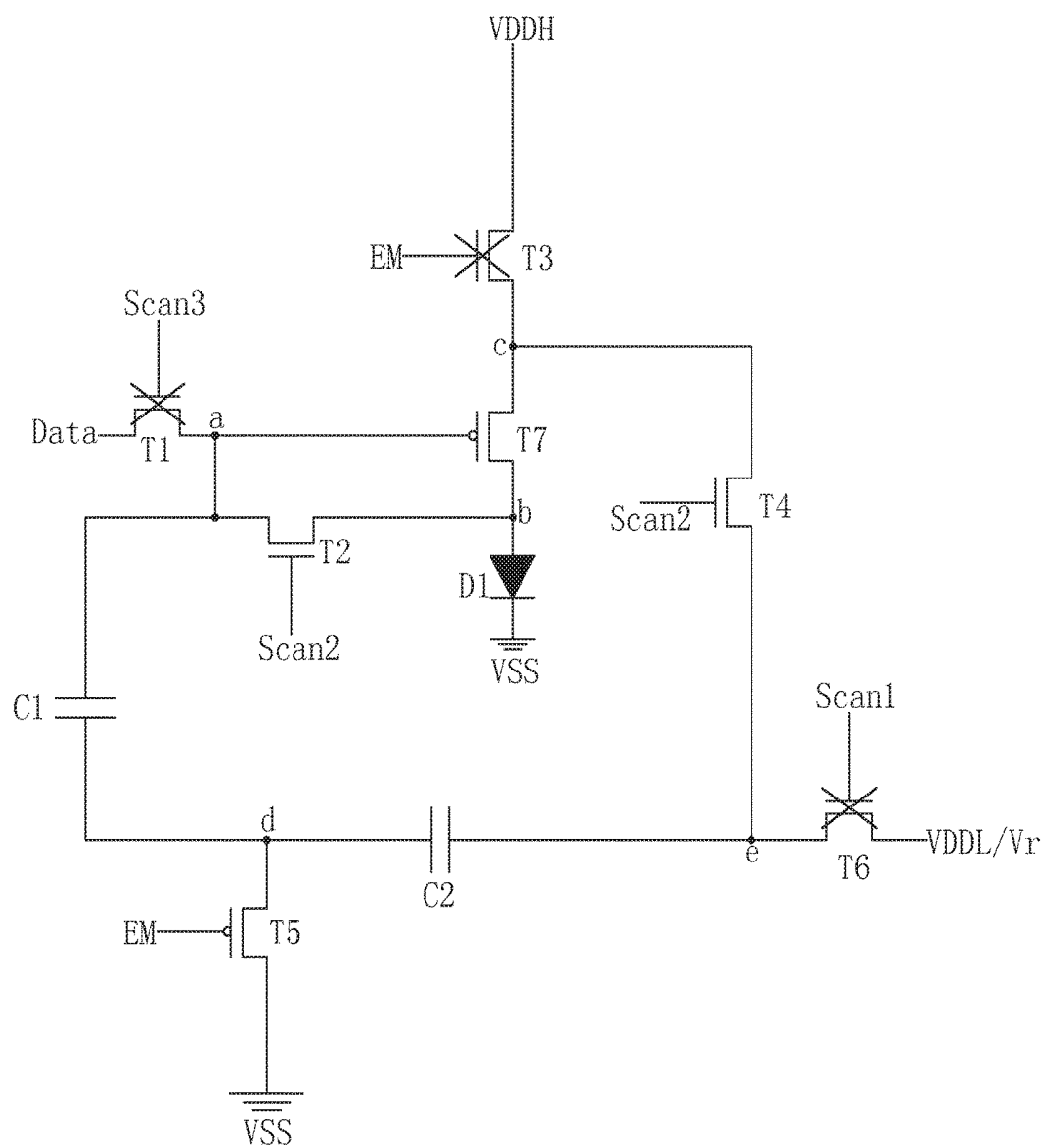


Fig. 5

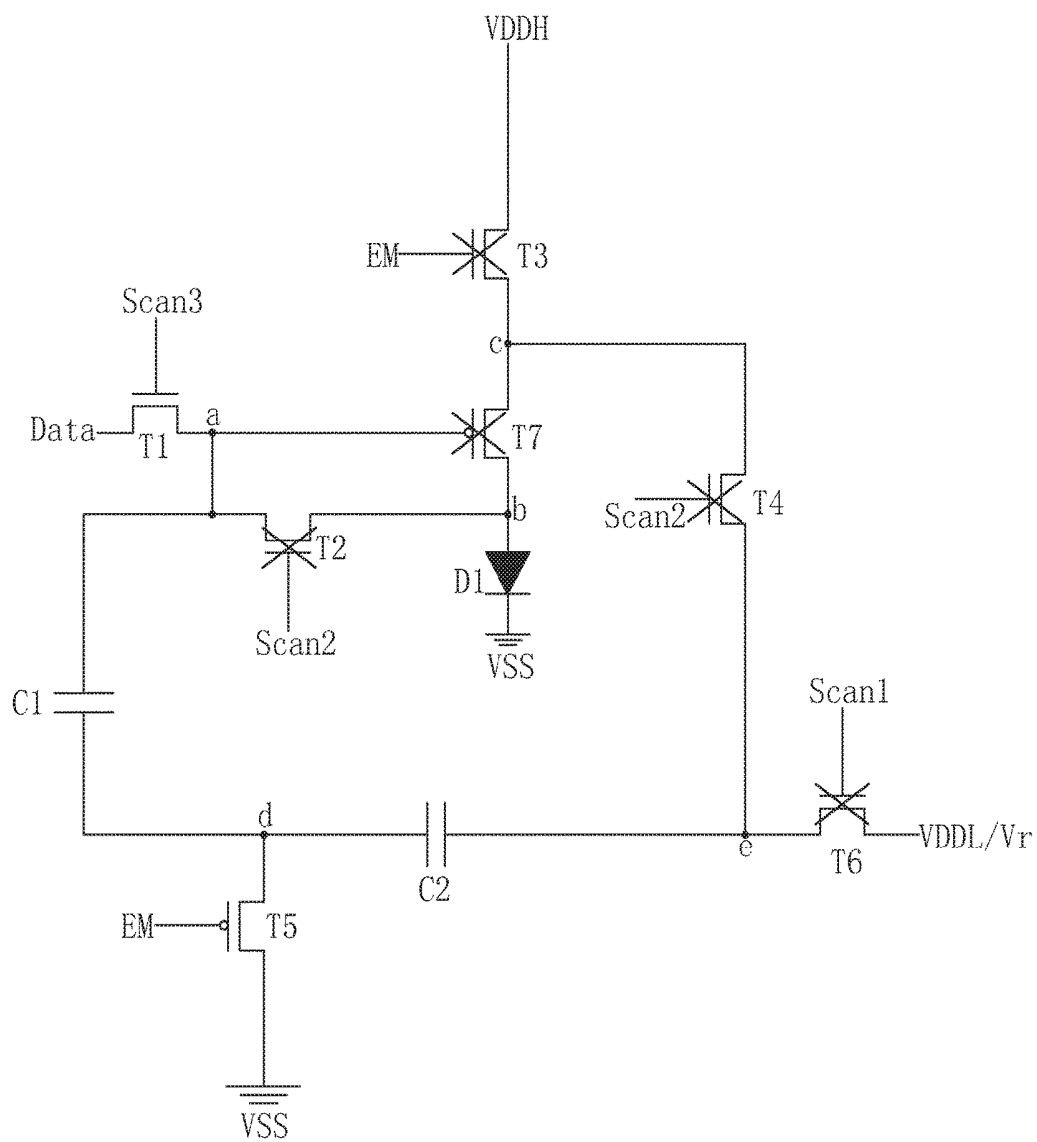


Fig. 6

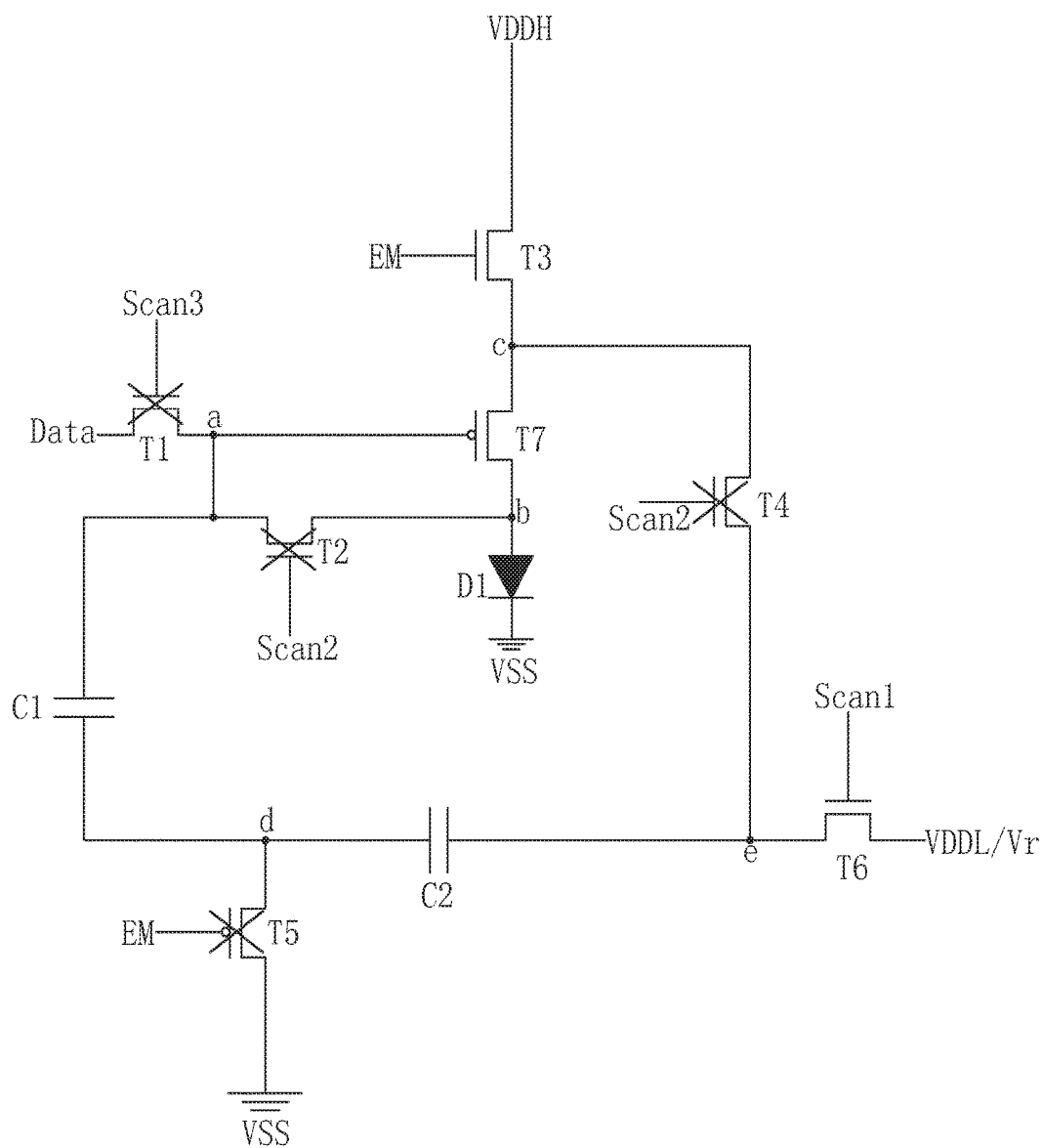


Fig. 7

OLED PIXEL DRIVING CIRCUIT AND PIXEL DRIVING METHOD

FIELD OF THE INVENTION

[0001] The present invention relates to a display technology field, and more particularly to an OLED pixel driving circuit and a pixel driving method.

BACKGROUND OF THE INVENTION

[0002] The Organic Light Emitting Display (OLED) possesses many outstanding properties of self-illumination, low driving voltage, high luminescence efficiency, short response time, high clarity and contrast, near 180° view angle, wide range of working temperature, applicability of flexible display and large scale full color display. The OLED is considered as the most potential display device.

[0003] The OLED is a current driving element. When the electrical current flows through the organic light emitting diode, the organic light emitting diode emits light, and the brightness is determined according to the current flowing through the organic light emitting diode itself. Most of the present Integrated Circuits (IC) only transmit voltage signals. Therefore, the OLED pixel driving circuit needs to accomplish the task of converting the voltage signals into the current signals. The traditional OLED pixel driving circuit generally is 2T1C, which is a structure comprising two thin film transistors and one capacitor to convert the voltage into the current.

[0004] As shown in FIG. 1, the traditional 2T1C pixel driving circuit used for OLED comprises: a first thin film transistor T10, a second thin film transistor T20 and a capacitor C10. The first thin film transistor T10 is a N type thin film transistor, which is used to be a switch thin film transistor; the second thin film transistor T20 is a P type thin film transistor, which is used to be a driving thin film transistor; the capacitor C10 is a storage capacitor. Specifically, a gate of the first thin film transistor T10 receives a scan signal Scan, and a source receives a data signal Data, and a drain is electrically coupled to the gate of the second thin film transistor T20 and one end of the capacitor C10; a source of the second thin film transistor T20 receives a power source voltage VDD, and a drain is electrically coupled to an anode of the organic light emitting diode D10; a cathode of the organic light emitting diode D10 receives a common ground voltage VSS; one end of the capacitor C10 is electrically coupled to a gate of the second thin film transistor T20, and the other end is electrically coupled to a source of the second thin film transistor T20. As the OLED displays, the scan signal Scan controls the first thin film transistor T10 to be activated, and the data signal Data enters the gate of the second thin film transistor T20 and the capacitor C10 via the first thin film transistor T10. Then, the first thin film transistor T10 is deactivated. With the storage function of the capacitor C10, the gate voltage of the second thin film transistor T20 can remain to hold the data signal voltage to make the second thin film transistor T20 to be in the conducted state to drive the current to enter the organic light emitting diode D10 via the second thin film transistor T20 and to drive the organic light emitting diode D10 to emit light.

[0005] The formula of the current flowing through the thin film transistor and the organic light emitting diode according to calculation is:

$$I_{OLED} = K \times (V_{gs} - V_{th})^2$$

[0006] wherein I_{OLED} represents a current flowing through the driving thin film transistor and the organic light emitting diode, and K is an intrinsic conductive factor of the driving thin film transistor, and V_{gs} represents a voltage difference between the gate and the source of the driving thin film transistor, and V_{th} represents a threshold voltage of the driving thin film transistor. Accordingly, the value of the I_{OLED} is relevant with the threshold voltage V_{th} of the driving thin film transistor.

[0007] The structure of the foregoing traditional OLED pixel driving circuit is simpler and does not possess compensation function, and thus lots of defects exist, wherein the more obvious one is: due to the nonconsistency in the manufacture process of the thin film transistor, the threshold voltages of the driving thin film transistors of all pixels in the OLED display panel are not consistent; and the long period of working time will age the material of the driving thin film transistors to lead to the drifts of the threshold voltages of the driving thin film transistors and the to cause the phenomenon of the nonuniform OLED panel display.

SUMMARY OF THE INVENTION

[0008] An objective of the present invention is to provide an OLED pixel driving circuit, which can eliminate the influence of the threshold voltage of the driving thin film transistor to the current flowing through the organic light emitting diode to promote the OLED panel display uniformity.

[0009] Another objective of the present invention is to provide an OLED pixel driving method, which can eliminate the influence of the threshold voltage of the driving thin film transistor to the current flowing through the organic light emitting diode to promote the OLED panel display uniformity.

[0010] For realizing the aforesaid objectives, the present invention first provides an OLED pixel driving circuit, comprising a first N type thin film transistor, a second N type thin film transistor, a third N type thin film transistor, a fourth N type thin film transistor, a fifth P type thin film transistor, a sixth N type thin film transistor, a seventh P type thin film transistor, a first capacitor, a second capacitor and an organic light emitting diode; the seventh P type thin film transistor serving as a driving thin film transistor of the organic light emitting diode;

[0011] a gate of the first N type thin film transistor receiving a third scan signal, and a source receiving a data signal, and a drain being electrically coupled to a first node;

[0012] a gate of the second N type thin film transistor receiving a second scan signal, and a source being electrically coupled to the first node, and a drain being electrically coupled to a second node;

[0013] a gate of the third N type thin film transistor receiving a light emitting control signal, and a source receiving a power source high voltage, and a drain being electrically coupled to a third node;

[0014] a gate of the fourth N type thin film transistor receiving the second scan signal, and a source being electrically coupled to the third node, and a drain being electrically coupled to a fifth node;

[0015] a gate of the fifth P type thin film transistor receiving a light emitting control signal, and a source being electrically coupled to a fourth node, and a drain receiving a common ground voltage;

[0016] a gate of the sixth N type thin film transistor receiving a first scan signal, and a source being electrically coupled to the fifth node, and a drain time-share receiving a power source low voltage or a luminous brightness adjustment voltage;

[0017] a gate of the seventh P type thin film transistor being electrically coupled to the first node, and a source being electrically coupled to the third node, and a drain being electrically coupled to the second node;

[0018] an anode of the organic light emitting diode being electrically coupled to the second node, and a cathode receiving the common ground voltage;

[0019] one end of the first capacitor being electrically coupled to the first node, and the other end being electrically coupled to the fourth node;

[0020] one end of the second capacitor being electrically coupled to the fourth node, and the other end being electrically coupled to the fifth node.

[0021] The first scan signal, the second scan signal, the third scan signal, the light emitting control signal, and the data signal are combined with one another to correspond to a reset stage, a threshold voltage detection stage, a program stage and a light emitting stage one after another.

[0022] in the reset stage, the first scan signal is a high voltage level, and the second scan signal is a low voltage level, and the third scan signal is a low voltage level, and the light emitting control signal is a low voltage level, and the data signal is a low voltage level; the drain of the sixth N type thin film transistor receives the power source low voltage;

[0023] in the threshold voltage detection stage, the first scan signal is a high voltage level, and the second scan signal is a low voltage level, and the light emitting control signal is a low voltage level, and the data signal is a low voltage level;

[0024] in the program stage, the first scan signal is a low voltage level, and the second scan signal is a low voltage level, and the third scan signal is a high voltage level, and the light emitting control signal is a low voltage level, and the data signal is a high voltage level;

[0025] in the light emitting stage, the first scan signal is a high voltage level, and the second scan signal is a low voltage level, and the third scan signal is a low voltage level, and the light emitting control signal is a high voltage level, and the data signal is a low voltage level; the drain of the sixth N type thin film transistor receives the luminous brightness adjustment voltage;

[0026] The power source low voltage is higher than a sum of a threshold voltage of the seventh P type thin film transistor and a threshold voltage of the organic light emitting diode.

[0027] The common ground voltage is not higher than the luminous brightness adjustment voltage, and the luminous brightness adjustment voltage is lower than a sum of the power source high voltage and the threshold voltage of the organic light emitting diode minus a voltage value of a high voltage level provided by the data signal.

[0028] All of the first scan signal, the second scan signal, the third scan signal, the light emitting control signal and the data signal are generated by an external sequence controller.

[0029] all of the first N type thin film transistor, the second N type thin film transistor, the third N type thin film transistor, the fourth N type thin film transistor, the fifth P type thin film transistor, the sixth N type thin film transistor, the seventh P type thin film transistor are low temperature poly-silicon thin film transistors, oxide semiconductor thin film transistors or amorphous silicon thin film transistors.

[0030] The present invention further provides an OLED pixel driving method, comprising steps of:

[0031] step 1, providing an OLED pixel driving circuit;

[0032] the OLED pixel driving circuit comprising a first N type thin film transistor, a second N type thin film transistor, a third N type thin film transistor, a fourth N type thin film transistor, a fifth P type thin film transistor, a sixth N type thin film transistor, a seventh P type thin film transistor, a first capacitor, a second capacitor and an organic light emitting diode; the seventh P type thin film transistor serving as a driving thin film transistor of the organic light emitting diode;

[0033] a gate of the first N type thin film transistor receiving a third scan signal, and a source receiving a data signal, and a drain being electrically coupled to a first node;

[0034] a gate of the second N type thin film transistor receiving a second scan signal, and a source being electrically coupled to the first node, and a drain being electrically coupled to a second node;

[0035] a gate of the third N type thin film transistor receiving a light emitting control signal, and a source receiving a power source high voltage, and a drain being electrically coupled to a third node;

[0036] a gate of the fourth N type thin film transistor receiving the second scan signal, and a source being electrically coupled to the third node, and a drain being electrically coupled to a fifth node;

[0037] a gate of the fifth P type thin film transistor receiving a light emitting control signal, and a source being electrically coupled to a fourth node, and a drain receiving a common ground voltage;

[0038] a gate of the sixth N type thin film transistor receiving a first scan signal, and a source being electrically coupled to the fifth node, and a drain time-share receiving a power source low voltage or a luminous brightness adjustment voltage;

[0039] a gate of the seventh P type thin film transistor being electrically coupled to the first node, and a source being electrically coupled to the third node, and a drain being electrically coupled to the second node;

[0040] an anode of the organic light emitting diode being electrically coupled to the second node, and a cathode receiving the common ground voltage;

[0041] one end of the first capacitor being electrically coupled to the first node, and the other end being electrically coupled to the fourth node;

[0042] one end of the second capacitor being electrically coupled to the fourth node, and the other end being electrically coupled to the fifth node;

[0043] step 2, entering a reset stage;

[0044] the first scan signal providing a high voltage level, and the second scan signal providing a low voltage level, and the third scan signal providing a low voltage level, and the light emitting control signal providing a low voltage level, and the data signal providing a low voltage level; the drain of the sixth N type thin film transistor receiving the power source low voltage;

[0045] the fifth P type thin film transistor and the sixth N type thin film transistor being on, and the other thin film transistors being off, and the power source low voltage charging the second capacitor to perform initializing assignment to the second capacitor, and resetting a voltage difference of two ends of the second capacitor to be VDDL-VSS, wherein VDDL represents the power source low voltage, and VSS represents the common ground voltage;

[0046] step 3, entering a threshold voltage detection stage;

[0047] the first scan signal being changed to be a low voltage level, and the second scan signal being changed to be a high voltage level, and the third scan signal being kept to be a low voltage level, and the light emitting control signal being kept to be a low voltage level, and the data signal being kept to be a low voltage level;

[0048] all of the second N type thin film transistor, the fourth N type thin film transistor, the fifth P type thin film transistor and the seventh P type thin film transistor being on, and all of the first N type thin film transistor, the third N type thin film transistor and the sixth N type thin film transistor being off, and the second capacitor being discharged to the seventh P type thin film transistor until an energy storage voltage of the second capacitor is $V_{th} + V_{th_OLED}$, wherein V_{th} is a threshold voltage of the seventh P type thin film transistor, and V_{th_OLED} is a threshold voltage of the organic light emitting diode;

[0049] step 4, entering a program stage;

[0050] the first scan signal being kept to be a low voltage level, and the second scan signal being changed to be a low voltage level, and the third scan signal being changed to be a high voltage level, and the light emitting diode control signal being kept to be a low voltage level, and the data signal being changed to be a high voltage level;

[0051] the first N type thin film transistor and the fifth P type thin film transistor being on, and the other thin film transistors being off, and the data signal charging the first capacitor until an energy storage voltage of the first capacitor and a voltage level of the first node are V_{Data} , and V_{Data} is a voltage value of a high voltage level provided by the data signal;

[0052] step 5, entering a light emitting stage;

[0053] the first scan signal being changed to be a high voltage level, and the second scan signal being kept to be a low voltage level, and the third scan signal being changed to be a low voltage level, and the light emitting control signal being changed to be a high voltage level, and the data signal being changed to be a low voltage level; the drain of the sixth N type thin film transistor receiving the luminous brightness adjustment voltage;

[0054] all of the third N type thin film transistor, the sixth N type thin film transistor and the fifth P type thin film transistor being on, and all of the first N type thin film transistor, the second N type thin film transistor, the fourth N type thin film transistor and the fifth P type thin film transistor being off, and the luminous brightness adjustment voltage being sent to the fifth node, and the voltage level of the first node being changed to be:

$$V_a = V_r + V_{Data} - V_{th} - V_{th_OLED}$$

[0055] wherein V_a represents a voltage level of the first node, and V_r represents the luminous brightness adjustment voltage;

[0056] the organic light emitting diode emits light, and a current flowing through the organic light emitting diode is irrelevant with the threshold voltage of the seventh P type thin film transistor.

[0057] The power source low voltage is higher than a sum of a threshold voltage of the seventh P type thin film transistor and a threshold voltage of the organic light emitting diode.

[0058] The common ground voltage is not higher than the luminous brightness adjustment voltage, and the luminous brightness adjustment voltage is lower than a sum of the power source high voltage and the threshold voltage of the organic light emitting diode minus a voltage value of a high voltage level provided by the data signal.

[0059] All of the first scan signal, the second scan signal, the third scan signal, the light emitting control signal and the data signal are generated by an external sequence controller;

[0060] all of the first N type thin film transistor, the second N type thin film transistor, the third N type thin film transistor, the fourth N type thin film transistor, the fifth P type thin film transistor, the sixth N type thin film transistor, the seventh P type thin film transistor are low temperature poly-silicon thin film transistors, oxide semiconductor thin film transistors or amorphous silicon thin film transistors.

[0061] The present invention further provides an OLED pixel driving circuit, comprising a first N type thin film transistor, a second N type thin film transistor, a third N type thin film transistor, a fourth N type thin film transistor, a fifth P type thin film transistor, a sixth N type thin film transistor, a seventh P type thin film transistor, a first capacitor, a second capacitor and an organic light emitting diode; the seventh P type thin film transistor serving as a driving thin film transistor of the organic light emitting diode;

[0062] a gate of the first N type thin film transistor receiving a third scan signal, and a source receiving a data signal, and a drain being electrically coupled to a first node;

[0063] a gate of the second N type thin film transistor receiving a second scan signal, and a source being electrically coupled to the first node, and a drain being electrically coupled to a second node;

[0064] a gate of the third N type thin film transistor receiving a light emitting control signal, and a source receiving a power source high voltage, and a drain being electrically coupled to a third node;

[0065] a gate of the fourth N type thin film transistor receiving the second scan signal, and a source being electrically coupled to the third node, and a drain being electrically coupled to a fifth node;

[0066] a gate of the fifth P type thin film transistor receiving a light emitting control signal, and a source being electrically coupled to a fourth node, and a drain receiving a common ground voltage;

[0067] a gate of the sixth N type thin film transistor receiving a first scan signal, and a source being electrically coupled to the fifth node, and a drain time-share receiving a power source low voltage or a luminous brightness adjustment voltage;

[0068] a gate of the seventh P type thin film transistor being electrically coupled to the first node, and a source being electrically coupled to the third node, and a drain being electrically coupled to the second node;

[0069] an anode of the organic light emitting diode being electrically coupled to the second node, and a cathode receiving the common ground voltage;

[0070] one end of the first capacitor being electrically coupled to the first node, and the other end being electrically coupled to the fourth node;

[0071] one end of the second capacitor being electrically coupled to the fourth node, and the other end being electrically coupled to the fifth node;

[0072] wherein the first scan signal, the second scan signal, the third scan signal, the light emitting control signal, and the data signal are combined with one another to correspond to a reset stage, a threshold voltage detection stage, a program stage and a light emitting stage one after another;

[0073] in the reset stage, the first scan signal is a high voltage level, and the second scan signal is a low voltage level, and the third scan signal is a low voltage level, and the light emitting control signal is a low voltage level, and the data signal is a low voltage level; the drain of the sixth N type thin film transistor receives the power source low voltage;

[0074] in the threshold voltage detection stage, the first scan signal is a high voltage level, and the second scan signal is a low voltage level, and the light emitting control signal is a low voltage level, and the data signal is a low voltage level;

[0075] in the program stage, the first scan signal is a low voltage level, and the second scan signal is a low voltage level, and the third scan signal is a high voltage level, and the light emitting control signal is a low voltage level, and the data signal is a high voltage level;

[0076] in the light emitting stage, the first scan signal is a high voltage level, and the second scan signal is a low voltage level, and the third scan signal is a low voltage level, and the light emitting control signal is a high voltage level, and the data signal is a low voltage level; the drain of the sixth N type thin film transistor receives the luminous brightness adjustment voltage;

[0077] wherein all of the first scan signal, the second scan signal, the third scan signal, the light emitting control signal and the data signal are generated by an external sequence controller.

[0078] The benefits of the present invention are: the present invention provides an OLED pixel driving circuit and a pixel driving method, which utilizes the pixel driving circuit of 7T2C structure, and the first scan signal, the second scan signal, the third scan signal, the light emitting control signal and the data signal are combined with one another to correspond to a reset stage, a threshold voltage detection stage, a program stage and a light emitting stage one after another and can eliminate the influence of the threshold voltage of the driving thin film transistor to the current flowing through the organic light emitting diode to promote the OLED panel display uniformity.

BRIEF DESCRIPTION OF THE DRAWINGS

[0079] In order to better understand the characteristics and technical aspect of the invention, please refer to the following detailed description of the present invention is concerned with the diagrams, however, provide reference to the accompanying drawings and description only and is not intended to be limiting of the invention.

[0080] In drawings,

[0081] FIG. 1 is a circuit diagram of a pixel driving circuit of traditional 2T1C structure;

[0082] FIG. 2 is a circuit diagram of an OLED pixel driving circuit according to the present invention;

[0083] FIG. 3 is a sequence diagram of an OLED pixel driving circuit according to present invention;

[0084] FIG. 4 is a circuit diagram of an OLED pixel driving circuit in a reset stage, and also a circuit diagram of step 2 in the OLED pixel driving method according to the present invention;

[0085] FIG. 5 is a circuit diagram of an OLED pixel driving circuit in a threshold voltage detection stage, and also a circuit diagram of step 3 in the OLED pixel driving method according to the present invention;

[0086] FIG. 6 is a circuit diagram of an OLED pixel driving circuit in a program stage, and also a circuit diagram of step 4 in the OLED pixel driving method according to the present invention;

[0087] FIG. 7 is a circuit diagram of an OLED pixel driving circuit in a light emitting stage, and also a circuit diagram of step 5 in the OLED pixel driving method according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0088] For better explaining the technical solution and the effect of the present invention, the present invention will be further described in detail with the accompanying drawings and the specific embodiments.

[0089] Please refer to FIG. 2 and FIG. 3. The present invention first provides an OLED pixel driving circuit, which utilizes the 7T2C structure and comprises a first N type thin film transistor T1, a second N type thin film transistor T2, a third N type thin film transistor T3, a fourth N type thin film transistor T4, a fifth P type thin film transistor T5, a sixth N type thin film transistor T6, a seventh P type thin film transistor T7, a first capacitor C1, a second capacitor C2 and an organic light emitting diode D1.

[0090] A gate of the first N type thin film transistor T1 receives a third scan signal Scan3, and a source receives a data signal Data, and a drain is electrically coupled to a first node a; a gate of the second N type thin film transistor T2 receives a second scan signal Scan2, and a source is electrically coupled to the first node a, and a drain is electrically coupled to a second node b; a gate of the third N type thin film transistor T3 receives a light emitting control signal EM, and a source receives a power source high voltage VDDH, and a drain is electrically coupled to a third node c; a gate of the fourth N type thin film transistor T4 receives the second scan signal Scan2, and a source is electrically coupled to the third node c, and a drain is electrically coupled to a fifth node e; a gate of the fifth P type thin film transistor T5 receives a light emitting control signal EM, and a source is electrically coupled to a fourth node d, and a drain receives a common ground voltage VSS; a gate of the sixth N type thin film transistor T6 receives a first scan signal Scan1, and a source is electrically coupled to the fifth node e, and a drain time-share receives a power source low voltage VDDL or a luminous brightness adjustment voltage Vr; the seventh P type thin film transistor T7 is a driving thin film transistor which directly drives the organic light emitting diode D1, of which a gate is electrically coupled to the first node a, and a source is electrically coupled to the third node c, and a drain is electrically coupled to the second node b; an anode of the organic light emitting diode D1 is electrically coupled to the second node b, and a cathode

receives the common ground voltage VSS; one end of the first capacitor C1 is electrically coupled to the first node a, and the other end is electrically coupled to the fourth node d; one end of the second capacitor C2 is electrically coupled to the fourth node d, and the other end is electrically coupled to the fifth node e.

[0091] Specifically, all of the first N type thin film transistor T1, the second N type thin film transistor T2, the third N type thin film transistor T3, the fourth N type thin film transistor T4, the fifth P type thin film transistor T5, the sixth N type thin film transistor T6 and the seventh P type thin film transistor T7 are low temperature poly-silicon thin film transistors, oxide semiconductor thin film transistors or amorphous silicon thin film transistors; all of the first scan signal Scan1, the second scan signal Scan2, the third scan signal Scan3, the light emitting control signal EM and the data signal Data are generated by an external sequence controller.

[0092] The first scan signal Scan1, the second scan signal Scan2, the third scan signal Scan3, the light emitting control signal EM, and the data signal Data are combined with one another to correspond to a reset stage S1, a threshold voltage detection stage S2, a program stage S3 and a light emitting stage S4 one after another.

[0093] Furthermore, combining FIG. 3 and FIG. 4, in the reset stage S1:

[0094] the first scan signal Scan1 is a high voltage level, and the second scan signal Scan2 is a low voltage level, and the third scan signal Scan3 is a low voltage level, and the light emitting control signal EM is a low voltage level, and the data signal Data is a low voltage level; the drain of the sixth N type thin film transistor T6 receives the power source low voltage VDDL.

[0095] The fifth P type thin film transistor T5 and the sixth N type thin film transistor T6 is on, and the other thin film transistors is off, and the power source low voltage VDDL charges the second capacitor C2 via the sixth N type thin film transistor T6 which is on, and a voltage difference of two ends of the second capacitor C2 after charging is accomplished, i.e. a voltage difference V_{ed} between the fifth node e and the fourth node d is:

$$V_{ed} = VDDL - V_{SS}$$

[0096] to accomplish the reset and initializing assignment to the second capacitor C2.

[0097] Significantly, the power source low voltage VDDL is higher than a sum of a threshold voltage of the seventh P type thin film transistor T7 and a threshold voltage of the organic light emitting diode D1, i.e.:

$$VDDL > V_{th} + V_{th_OLED}$$

[0098] wherein V_{th} represents a threshold voltage of the seventh P type thin film transistor T7, and V_{th_OLED} is a threshold voltage of the organic light emitting diode D1.

[0099] Combining FIG. 3 and FIG. 5, in the threshold voltage detection stage S2:

[0100] in the threshold voltage detection stage S2, the first scan signal Scan1 is a low voltage level, and the second scan signal Scan2 is a high voltage level, and the third scan signal Scan3 is a low voltage level, and the light emitting control signal EM is a low voltage level, and the data signal Data is a low voltage level.

[0101] All of the second N type thin film transistor T2, the fourth N type thin film transistor T4, the fifth P type thin film transistor T5 and the seventh P type thin film transistor T7

are on, and all of the first N type thin film transistor T1, the third N type thin film transistor T3 and the sixth N type thin film transistor T6 are off, and the fifth node e is coupled with the third node c, i.e. the source of the seventh P type thin film transistor T7 via the fourth N type thin film transistor T4 which is on, and the first node a, i.e. the gate of the seventh P type thin film transistor T7 is coupled to the second node b, i.e. the anode of the organic light emitting diode D1 via the second N type thin film transistor T2 which is on, and the second capacitor C2 is discharged to the seventh P type thin film transistor T7 until a voltage difference V_{ed} between the fifth node e and the fourth node d is:

$$V_{ed} = V_{th} + V_{th_OLED}$$

[0102] then, an energy storage voltage of the second capacitor C2 is $V_{th} + V_{th_OLED}$.

[0103] Combining FIG. 3 and FIG. 6, in the program stage S3:

[0104] the first scan signal Scan1 is a low voltage level, and the second scan signal Scan2 is a low voltage level, and the third scan signal Scan3 is a high voltage level, and the light emitting control signal EM is a low voltage level, and the data signal Data is a high voltage level.

[0105] The first N type thin film transistor T1 and the fifth P type thin film transistor T5 are on, and the other thin film transistors are off, and the data signal charges the first capacitor C1 via the first N type thin film transistor T1 until an energy storage voltage of the first capacitor C1 and a voltage level of the first node a are a voltage value V_{Data} of a high voltage level provided by the data signal Data.

[0106] In the program stage S3, the second capacitor C2 is in a floating state.

[0107] Combining FIG. 3 and FIG. 7, in the light emitting stage S4:

[0108] the first scan signal Scan1 is a high voltage level, and the second scan signal Scan2 is a low voltage level, and the third scan signal Scan3 is a low voltage level, and the light emitting control signal EM is a high voltage level, and the data signal Data is a low voltage level; the drain of the sixth N type thin film transistor T6 receives the luminous brightness adjustment voltage Vr.

[0109] All of the third N type thin film transistor T3, the sixth N type thin film transistor T6 and the seventh P type thin film transistor T7 are on, and all of the first N type thin film transistor T1, the second N type thin film transistor T2, the fourth N type thin film transistor T4 and the fifth P type thin film transistor T5 are off, and the luminous brightness adjustment voltage Vr is sent to the fifth node e via the sixth N type thin film transistor T6, and the voltage level Va of the first node a, i.e. a gate voltage level of the seventh P type thin film transistor T7 is changed to be:

$$V_a = V_r + (V_{Data} - (V_{th} + V_{th_OLED})) = V_r + V_{Data} - V_{th} - V_{th_OLED}$$

[0110] the power source high voltage level VDDH is sent to the third node c, i.e. the source of the seventh P type thin film transistor T7 via the third N type thin film transistor T3 which is on:

$$V_c = VDDH$$

[0111] wherein Vc represents a voltage of the third node c, i.e. the source of the seventh P type thin film transistor T7.

[0112] The formula of the current flowing through the P type thin film transistor and the organic light emitting diode according to calculation is:

$$\begin{aligned}
I_{OLED} &= K \times (V_c - V_a - V_{th})^2 \\
&= K \times (VDDH - (V_r + V_{Data} - V_{th} - V_{th_OLED}) - V_{th})^2 \\
&= K \times (VDDH - V_r - V_{Data} + V_{th_OLED})^2
\end{aligned}$$

[0113] wherein I_{OLED} represents a current flowing through the driving thin film transistor, i.e. the seventh P type thin film transistor T7 and the organic light emitting diode D1, and K is an intrinsic conductive factor of the driving thin film transistor, i.e. the seventh P type thin film transistor T7.

[0114] The organic light emitting diode D1 emits light, and the current I_{OLED} flowing through the organic light emitting diode D1 is irrelevant with the threshold voltage V_{th} of the seventh P type thin film transistor T7, which can eliminate the influence of the threshold voltage of the driving thin film transistor to the current flowing through the organic light emitting diode to promote the OLED panel display uniformity.

[0115] Significantly, the common ground voltage VSS is not higher than the luminous brightness adjustment voltage V_r , and the luminous brightness adjustment voltage V_r is lower than a sum of the power source high voltage VDDH and the threshold voltage V_{th_OLED} of the organic light emitting diode D1 minus a voltage value V_{Data} of a high voltage level provided by the data signal Data.

$$VSS \leq V_r < VDDH - V_{Data} + V_{th_OLED}$$

[0116] Besides, the above expression formula for calculating I_{OLED} , $I_{OLED} = K \times (VDDH - V_r - V_{Data} + V_{th_OLED})^2$ contains the item of threshold voltage V_{th_OLED} of the organic light emitting diode D1. Since the organic light emitting diode D1 will age after a long time usage so that the threshold voltage V_{th_OLED} of the organic light emitting diode D1 rises to result in the decrease of the luminous efficiency. However, it can be told from the expression formula of I_{OLED} that the rising V_{th_OLED} makes the current I_{OLED} flowing through the organic light emitting diode D1 increase, and the increased current can compensate the decreased luminous efficiency for solving the issue of the decreased luminous efficiency.

[0117] On the basis of the same inventive idea, the present invention further provides an OLED pixel driving method, comprising steps of:

[0118] step 1, providing an OLED pixel driving circuit.

[0119] As shown in FIG. 2, the OLED pixel driving circuit utilizes the 7T2C structure and comprises a first N type thin film transistor T1, a second N type thin film transistor T2, a third N type thin film transistor T3, a fourth N type thin film transistor T4, a fifth P type thin film transistor T5, a sixth N type thin film transistor T6, a seventh P type thin film transistor T7, a first capacitor C1, a second capacitor C2 and an organic light emitting diode D1.

[0120] A gate of the first N type thin film transistor T1 receives a third scan signal Scan3, and a source receives a data signal Data, and a drain is electrically coupled to a first node a; a gate of the second N type thin film transistor T2 receives a second scan signal Scan2, and a source is electrically coupled to the first node a, and a drain is electrically coupled to a second node b; a gate of the third N type thin film transistor T3 receives a light emitting control signal EM, and a source receives a power source high voltage VDDH, and a drain is electrically coupled to a third node c;

a gate of the fourth N type thin film transistor T4 receives the second scan signal Scan2, and a source is electrically coupled to the third node c, and a drain is electrically coupled to a fifth node e; a gate of the fifth P type thin film transistor T5 receives a light emitting control signal EM, and a source is electrically coupled to a fourth node d, and a drain receives a common ground voltage VSS; a gate of the sixth N type thin film transistor T6 receives a first scan signal Scan1, and a source is electrically coupled to the fifth node e, and a drain time-share receives a power source low voltage VDDL or a luminous brightness adjustment voltage V_r ; the seventh P type thin film transistor T7 is a driving thin film transistor which directly drives the organic light emitting diode D1, of which a gate is electrically coupled to the first node a, and a source is electrically coupled to the third node c, and a drain is electrically coupled to the second node b; an anode of the organic light emitting diode D1 is electrically coupled to the second node b, and a cathode receives the common ground voltage VSS; one end of the first capacitor C1 is electrically coupled to the first node a, and the other end is electrically coupled to the fourth node d; one end of the second capacitor C2 is electrically coupled to the fourth node d, and the other end is electrically coupled to the fifth node e.

[0121] Specifically, all of the first N type thin film transistor T1, the second N type thin film transistor T2, the third N type thin film transistor T3, the fourth N type thin film transistor T4, the fifth P type thin film transistor T5, the sixth N type thin film transistor T6 and the seventh P type thin film transistor T7 are low temperature poly-silicon thin film transistors, oxide semiconductor thin film transistors or amorphous silicon thin film transistors; all of the first scan signal Scan1, the second scan signal Scan2, the third scan signal Scan3, the light emitting control signal EM and the data signal Data are generated by an external sequence controller.

[0122] step 2, referring to FIG. 3 and FIG. 4, together, entering the reset stage 51.

[0123] The first scan signal Scan1 provides a high voltage level, and the second scan signal Scan2 provides a low voltage level, and the third scan signal Scan3 provides a low voltage level, and the light emitting control signal EM provides a low voltage level, and the data signal Data provides a low voltage level; the drain of the sixth N type thin film transistor T6 receives the power source low voltage VDDL.

[0124] The fifth P type thin film transistor T5 and the sixth N type thin film transistor T6 is on, and the other thin film transistors is off, and the power source low voltage VDDL charges the second capacitor C2 via the sixth N type thin film transistor T6 which is on, and a voltage difference of two ends of the second capacitor C2 after charging is accomplished, i.e. a voltage difference V_{ed} between the fifth node e and the fourth node d is:

$$V_{ed} = VDDL - VSS$$

[0125] to accomplish the reset and initializing assignment to the second capacitor C2.

[0126] Significantly, the power source low voltage VDDL is higher than a sum of a threshold voltage of the seventh P type thin film transistor T7 and a threshold voltage of the organic light emitting diode D1, i.e.:

$$VDDL > V_{th} + V_{th_OLED}$$

[0127] wherein V_{th} represents a threshold voltage of the seventh P type thin film transistor T7, and V_{th_OLED} is a threshold voltage of the organic light emitting diode D1.

[0128] step 3, Combining FIG. 3 and FIG. 5, entering the threshold voltage detection stage S2.

[0129] The first scan signal Scan1 is changed to be a low voltage level, and the second scan signal Scan2 is changed to be a high voltage level, and the third scan signal Scan3 is kept to be a low voltage level, and the light emitting control signal EM is kept to be a low voltage level, and the data signal Data is kept to be a low voltage level.

[0130] All of the second N type thin film transistor T2, the fourth N type thin film transistor T4, the fifth P type thin film transistor T5 and the seventh P type thin film transistor T7 are on, and all of the first N type thin film transistor T1, the third N type thin film transistor T3 and the sixth N type thin film transistor T6 are off, and the fifth node e is coupled with the third node c, i.e. the source of the seventh P type thin film transistor T7 via the fourth N type thin film transistor T4 which is on, and the first node a, i.e. the gate of the seventh P type thin film transistor T7 is coupled to the second node b, i.e. the anode of the organic light emitting diode D1 via the second N type thin film transistor T2 which is on, and the second capacitor C2 is discharged to the seventh P type thin film transistor T7 until a voltage difference V_{ed} between the fifth node e and the fourth node d is:

$$V_{ed} = V_{th} + V_{th_OLED}$$

[0131] then, an energy storage voltage of the second capacitor C2 is $V_{th} + V_{th_OLED}$.

[0132] step 4, combining FIG. 3 and FIG. 6, entering the program stage S3.

[0133] The first scan signal Scan1 is kept to be a low voltage level, and the second scan signal Scan2 is changed to be a low voltage level, and the third scan signal Scan3 is changed to be a high voltage level, and the light emitting diode control signal EM is kept to be a low voltage level, and the data signal Data is changed to be a high voltage level.

[0134] The first N type thin film transistor T1 and the fifth P type thin film transistor T5 are on, and the other thin film transistors are off, and the data signal charges the first capacitor C1 via the first N type thin film transistor T1 until an energy storage voltage of the first capacitor C1 and a voltage level of the first node a are a voltage value V_{Data} of a high voltage level provided by the data signal Data.

[0135] In the program stage S3, the second capacitor C2 is in a floating state.

[0136] step 5, combining FIG. 3 and FIG. 7, entering the light emitting stage S4.

[0137] the first scan signal Scan1 is changed to be a high voltage level, and the second scan signal Scan2 is kept to be a low voltage level, and the third scan signal Scan3 is changed to be a low voltage level, and the light emitting control signal EM is changed to be a high voltage level, and the data signal Data is changed to be a low voltage level; the drain of the sixth N type thin film transistor T6 receives the luminous brightness adjustment voltage Vr.

[0138] All of the third N type thin film transistor T3, the sixth N type thin film transistor T6 and the seventh P type thin film transistor T7 are on, and all of the first N type thin film transistor T1, the second N type thin film transistor T2, the fourth N type thin film transistor T4 and the fifth P type thin film transistor T5 are off, and the luminous brightness adjustment voltage Vr is sent to the fifth node e via the sixth

N type thin film transistor T6, and the voltage level Va of the first node a, i.e. a gate voltage level of the seventh P type thin film transistor T7 is changed to be:

$$V_a = V_r + (V_{Data} - (V_{th} + V_{th13_OLED})) = V_r + V_{Data} - V_{th} - V_{th_}$$

[0139] the power source high voltage level VDDH is sent to the third node c, i.e. the source of the seventh P type thin film transistor T7 via the third N type thin film transistor T3 which is on:

$$V_c = VDDH$$

[0140] wherein Vc represents a voltage of the third node c, i.e. the source of the seventh P type thin film transistor T7.

[0141] The formula of the current flowing through the P type thin film transistor and the organic light emitting diode according to calculation is:

$$\begin{aligned} I_{OLED} &= K \times (V_c - V_a - V_{th})^2 \\ &= K \times (VDDH - (V_r + V_{Data} - V_{th} - V_{th_OLED}) - V_{th})^2 \\ &= K \times (VDDH - V_r - V_{Data} + V_{th_OLED})^2 \end{aligned}$$

[0142] wherein I_{OLED} represents a current flowing through the driving thin film transistor, i.e. the seventh P type thin film transistor T7 and the organic light emitting diode D1, and K is an intrinsic conductive factor of the driving thin film transistor, i.e. the seventh P type thin film transistor T7.

[0143] The organic light emitting diode D1 emits light, and the current I_{OLED} flowing through the organic light emitting diode D1 is irrelevant with the threshold voltage V_{th} of the seventh P type thin film transistor T7, which can eliminate the influence of the threshold voltage of the driving thin film transistor to the current flowing through the organic light emitting diode to promote the OLED panel display uniformity.

[0144] Significantly, the common ground voltage VSS is not higher than the luminous brightness adjustment voltage Vr, and the luminous brightness adjustment voltage Vr is lower than a sum of the power source high voltage VDDH and the threshold voltage V_{th_OLED} of the organic light emitting diode D1 minus a voltage value V_{Data} of a high voltage level provided by the data signal Data.

$$VSS \leq V_r < VDDH - V_{Data} + V_{th_OLED}$$

[0145] Besides, the above expression formula for calculating I_{OLED} , $I_{OLED} = K \times (VDDH - V_r - V_{Data} + V_{th_OLED})^2$ contains the item of threshold voltage V_{th_OLED} of the organic light emitting diode D1. Since the organic light emitting diode D1 will age after a long time usage so that the threshold voltage V_{th_OLED} of the organic light emitting diode D1 rises to result in the decrease of the luminous efficiency. However, it can be told from the expression formula of I_{OLED} that the rising V_{th_OLED} makes the current I_{OLED} flowing through the organic light emitting diode D1 increase, and the increased current can compensate the decreased luminous efficiency for solving the issue of the decreased luminous efficiency.

[0146] In conclusion, the OLED pixel driving circuit and the pixel driving method of the present invention utilizes the pixel driving circuit of 7T2C structure, and the first scan signal, the second scan signal, the third scan signal, the light emitting control signal and the data signal are combined

with one another to correspond to a reset stage, a threshold voltage detection stage, a program stage and a light emitting stage one after another and can eliminate the influence of the threshold voltage of the driving thin film transistor to the current flowing through the organic light emitting diode to promote the OLED panel display uniformity.

[0147] Above are only specific embodiments of the present invention, the scope of the present invention is not limited to this, and to any persons who are skilled in the art, change or replacement which is easily derived should be covered by the protected scope of the invention. Thus, the protected scope of the invention should go by the subject claims.

What is claimed is:

1. An OLED pixel driving circuit, comprising a first N type thin film transistor, a second N type thin film transistor, a third N type thin film transistor, a fourth N type thin film transistor, a fifth P type thin film transistor, a sixth N type thin film transistor, a seventh P type thin film transistor, a first capacitor, a second capacitor and an organic light emitting diode; the seventh P type thin film transistor serving as a driving thin film transistor of the organic light emitting diode;

a gate of the first N type thin film transistor receiving a third scan signal, and a source receiving a data signal, and a drain being electrically coupled to a first node;

a gate of the second N type thin film transistor receiving a second scan signal, and a source being electrically coupled to the first node, and a drain being electrically coupled to a second node;

a gate of the third N type thin film transistor receiving a light emitting control signal, and a source receiving a power source high voltage, and a drain being electrically coupled to a third node;

a gate of the fourth N type thin film transistor receiving the second scan signal, and a source being electrically coupled to the third node, and a drain being electrically coupled to a fifth node;

a gate of the fifth P type thin film transistor receiving a light emitting control signal, and a source being electrically coupled to a fourth node, and a drain receiving a common ground voltage;

a gate of the sixth N type thin film transistor receiving a first scan signal, and a source being electrically coupled to the fifth node, and a drain time-share receiving a power source low voltage or a luminous brightness adjustment voltage;

a gate of the seventh P type thin film transistor being electrically coupled to the first node, and a source being electrically coupled to the third node, and a drain being electrically coupled to the second node;

an anode of the organic light emitting diode being electrically coupled to the second node, and a cathode receiving the common ground voltage;

one end of the first capacitor being electrically coupled to the first node, and the other end being electrically coupled to the fourth node;

one end of the second capacitor being electrically coupled to the fourth node, and the other end being electrically coupled to the fifth node.

2. The OLED pixel driving circuit according to claim 1, wherein the first scan signal, the second scan signal, the third scan signal, the light emitting control signal, and the data signal are combined with one another to correspond to a

reset stage, a threshold voltage detection stage, a program stage and a light emitting stage one after another.

in the reset stage, the first scan signal is a high voltage level, and the second scan signal is a low voltage level, and the third scan signal is a low voltage level, and the light emitting control signal is a low voltage level, and the data signal is a low voltage level; the drain of the sixth N type thin film transistor receives the power source low voltage;

in the threshold voltage detection stage, the first scan signal is a high voltage level, and the second scan signal is a low voltage level, and the light emitting control signal is a low voltage level, and the data signal is a low voltage level;

in the program stage, the first scan signal is a low voltage level, and the second scan signal is a low voltage level, and the third scan signal is a high voltage level, and the light emitting control signal is a low voltage level, and the data signal is a high voltage level;

in the light emitting stage, the first scan signal is a high voltage level, and the second scan signal is a low voltage level, and the third scan signal is a low voltage level, and the light emitting control signal is a high voltage level, and the data signal is a low voltage level; the drain of the sixth N type thin film transistor receives the luminous brightness adjustment voltage.

3. The OLED pixel driving circuit according to claim 1, wherein the power source low voltage is higher than a sum of a threshold voltage of the seventh P type thin film transistor and a threshold voltage of the organic light emitting diode.

4. The OLED pixel driving circuit according to claim 3, wherein the common ground voltage is not higher than the luminous brightness adjustment voltage, and the luminous brightness adjustment voltage is lower than a sum of the power source high voltage and the threshold voltage of the organic light emitting diode minus a voltage value of a high voltage level provided by the data signal.

5. The OLED pixel driving circuit according to claim 1, wherein all of the first scan signal, the second scan signal, the third scan signal, the light emitting control signal and the data signal are generated by an external sequence controller.

6. The OLED pixel driving circuit according to claim 1, wherein all of the first N type thin film transistor, the second N type thin film transistor, the third N type thin film transistor, the fourth N type thin film transistor, the fifth P type thin film transistor, the sixth N type thin film transistor, the seventh P type thin film transistor are low temperature poly-silicon thin film transistors, oxide semiconductor thin film transistors or amorphous silicon thin film transistors.

7. An OLED pixel driving method, comprising steps of: step 1, providing an OLED pixel driving circuit;

the OLED pixel driving circuit comprising a first N type thin film transistor, a second N type thin film transistor, a third N type thin film transistor, a fourth N type thin film transistor, a fifth P type thin film transistor, a sixth N type thin film transistor, a seventh P type thin film transistor, a first capacitor, a second capacitor and an organic light emitting diode; the seventh P type thin film transistor serving as a driving thin film transistor of the organic light emitting diode;

a gate of the first N type thin film transistor receiving a third scan signal, and a source receiving a data signal, and a drain being electrically coupled to a first node;

a gate of the second N type thin film transistor receiving a second scan signal, and a source being electrically coupled to the first node, and a drain being electrically coupled to a second node;

a gate of the third N type thin film transistor receiving a light emitting control signal, and a source receiving a power source high voltage, and a drain being electrically coupled to a third node;

a gate of the fourth N type thin film transistor receiving the second scan signal, and a source being electrically coupled to the third node, and a drain being electrically coupled to a fifth node;

a gate of the fifth P type thin film transistor receiving a light emitting control signal, and a source being electrically coupled to a fourth node, and a drain receiving a common ground voltage;

a gate of the sixth N type thin film transistor receiving a first scan signal, and a source being electrically coupled to the fifth node, and a drain time-share receiving a power source low voltage or a luminous brightness adjustment voltage;

a gate of the seventh P type thin film transistor being electrically coupled to the first node, and a source being electrically coupled to the third node, and a drain being electrically coupled to the second node;

an anode of the organic light emitting diode being electrically coupled to the second node, and a cathode receiving the common ground voltage;

one end of the first capacitor being electrically coupled to the first node, and the other end being electrically coupled to the fourth node;

one end of the second capacitor being electrically coupled to the fourth node, and the other end being electrically coupled to the fifth node;

step 2, entering a reset stage;

the first scan signal providing a high voltage level, and the second scan signal providing a low voltage level, and the third scan signal providing a low voltage level, and the light emitting control signal providing a low voltage level, and the data signal providing a low voltage level; the drain of the sixth N type thin film transistor receiving the power source low voltage;

the fifth P type thin film transistor and the sixth N type thin film transistor being on, and the other thin film transistors being off, and the power source low voltage charging the second capacitor to perform initializing assignment to the second capacitor, and resetting a voltage difference of two ends of the second capacitor to be $VDDL-VSS$, wherein $VDDL$ represents the power source low voltage, and VSS represents the common ground voltage;

step 3, entering a threshold voltage detection stage;

the first scan signal being changed to be a low voltage level, and the second scan signal being changed to be a high voltage level, and the third scan signal being kept to be a low voltage level, and the light emitting control signal being kept to be a low voltage level, and the data signal being kept to be a low voltage level;

all of the second N type thin film transistor, the fourth N type thin film transistor, the fifth P type thin film transistor and the seventh P type thin film transistor being on, and all of the first N type thin film transistor, the third N type thin film transistor and the sixth N type thin film transistor being off, and the second capacitor

being discharged to the seventh P type thin film transistor until an energy storage voltage of the second capacitor is $V_{th}+V_{th_OLED}$, wherein V_{th} is a threshold voltage of the seventh P type thin film transistor, and V_{th_OLED} is a threshold voltage of the organic light emitting diode;

step 4, entering a program stage;

the first scan signal being kept to be a low voltage level, and the second scan signal being changed to be a low voltage level, and the third scan signal being changed to be a high voltage level, and the light emitting diode control signal being kept to be a low voltage level, and the data signal being changed to be a high voltage level; the first N type thin film transistor and the fifth P type thin film transistor being on, and the other thin film transistors being off, and the data signal charging the first capacitor until an energy storage voltage of the first capacitor and a voltage level of the first node are V_{Data} , and V_{Data} is a voltage value of a high voltage level provided by the data signal;

step 5, entering a light emitting stage;

the first scan signal being changed to be a high voltage level, and the second scan signal being kept to be a low voltage level, and the third scan signal being changed to be a low voltage level, and the light emitting control signal being changed to be a high voltage level, and the data signal being changed to be a low voltage level; the drain of the sixth N type thin film transistor receiving the luminous brightness adjustment voltage;

all of the third N type thin film transistor, the sixth N type thin film transistor and the fifth P type thin film transistor being on, and all of the first N type thin film transistor, the second N type thin film transistor, the fourth N type thin film transistor and the fifth P type thin film transistor being off, and the luminous brightness adjustment voltage being sent to the fifth node, and the voltage level of the first node being changed to be:

$$V_a = V_r + V_{Data} - V_{th} - V_{th_OLED}$$

wherein V_a represents a voltage level of the first node, and V_r represents the luminous brightness adjustment voltage;

the organic light emitting diode emits light, and a current flowing through the organic light emitting diode is irrelevant with the threshold voltage of the seventh P type thin film transistor.

8. The OLED pixel driving method according to claim 7, wherein the power source low voltage is higher than a sum of a threshold voltage of the seventh P type thin film transistor and a threshold voltage of the organic light emitting diode.

9. The OLED pixel driving method according to claim 8, wherein the common ground voltage is not higher than the luminous brightness adjustment voltage, and the luminous brightness adjustment voltage is lower than a sum of the power source high voltage and the threshold voltage of the organic light emitting diode minus a voltage value of a high voltage level provided by the data signal.

10. The OLED pixel driving method according to claim 7, wherein all of the first scan signal, the second scan signal, the third scan signal, the light emitting control signal and the data signal are generated by an external sequence controller.

all of the first N type thin film transistor, the second N type thin film transistor, the third N type thin film transistor,

the fourth N type thin film transistor, the fifth P type thin film transistor, the sixth N type thin film transistor, the seventh P type thin film transistor are low temperature poly-silicon thin film transistors, oxide semiconductor thin film transistors or amorphous silicon thin film transistors.

11. An OLED pixel driving circuit, comprising a first N type thin film transistor, a second N type thin film transistor, a third N type thin film transistor, a fourth N type thin film transistor, a fifth P type thin film transistor, a sixth N type thin film transistor, a seventh P type thin film transistor, a first capacitor, a second capacitor and an organic light emitting diode; the seventh P type thin film transistor serving as a driving thin film transistor of the organic light emitting diode;

- a gate of the first N type thin film transistor receiving a third scan signal, and a source receiving a data signal, and a drain being electrically coupled to a first node;
 - a gate of the second N type thin film transistor receiving a second scan signal, and a source being electrically coupled to the first node, and a drain being electrically coupled to a second node;
 - a gate of the third N type thin film transistor receiving a light emitting control signal, and a source receiving a power source high voltage, and a drain being electrically coupled to a third node;
 - a gate of the fourth N type thin film transistor receiving the second scan signal, and a source being electrically coupled to the third node, and a drain being electrically coupled to a fifth node;
 - a gate of the fifth P type thin film transistor receiving a light emitting control signal, and a source being electrically coupled to a fourth node, and a drain receiving a common ground voltage;
 - a gate of the sixth N type thin film transistor receiving a first scan signal, and a source being electrically coupled to the fifth node, and a drain time-share receiving a power source low voltage or a luminous brightness adjustment voltage;
 - a gate of the seventh P type thin film transistor being electrically coupled to the first node, and a source being electrically coupled to the third node, and a drain being electrically coupled to the second node;
 - an anode of the organic light emitting diode being electrically coupled to the second node, and a cathode receiving the common ground voltage;
 - one end of the first capacitor being electrically coupled to the first node, and the other end being electrically coupled to the fourth node;
 - one end of the second capacitor being electrically coupled to the fourth node, and the other end being electrically coupled to the fifth node;
- wherein the first scan signal, the second scan signal, the third scan signal, the light emitting control signal, and the data signal are combined with one another to

correspond to a reset stage, a threshold voltage detection stage, a program stage and a light emitting stage one after another;

in the reset stage, the first scan signal is a high voltage level, and the second scan signal is a low voltage level, and the third scan signal is a low voltage level, and the light emitting control signal is a low voltage level, and the data signal is a low voltage level; the drain of the sixth N type thin film transistor receives the power source low voltage;

in the threshold voltage detection stage, the first scan signal is a high voltage level, and the second scan signal is a low voltage level, and the light emitting control signal is a low voltage level, and the data signal is a low voltage level;

in the program stage, the first scan signal is a low voltage level, and the second scan signal is a low voltage level, and the third scan signal is a high voltage level, and the light emitting control signal is a low voltage level, and the data signal is a high voltage level;

in the light emitting stage, the first scan signal is a high voltage level, and the second scan signal is a low voltage level, and the third scan signal is a low voltage level, and the light emitting control signal is a high voltage level, and the data signal is a low voltage level; the drain of the sixth N type thin film transistor receives the luminous brightness adjustment voltage;

wherein all of the first scan signal, the second scan signal, the third scan signal, the light emitting control signal and the data signal are generated by an external sequence controller.

12. The OLED pixel driving circuit according to claim 11, wherein the power source low voltage is higher than a sum of a threshold voltage of the seventh P type thin film transistor and a threshold voltage of the organic light emitting diode.

13. The OLED pixel driving circuit according to claim 12, wherein the common ground voltage is not higher than the luminous brightness adjustment voltage, and the luminous brightness adjustment voltage is lower than a sum of the power source high voltage and the threshold voltage of the organic light emitting diode minus a voltage value of a high voltage level provided by the data signal.

14. The OLED pixel driving circuit according to claim 11, wherein all of the first N type thin film transistor, the second N type thin film transistor, the third N type thin film transistor, the fourth N type thin film transistor, the fifth P type thin film transistor, the sixth N type thin film transistor, the seventh P type thin film transistor are low temperature poly-silicon thin film transistors, oxide semiconductor thin film transistors or amorphous silicon thin film transistors.

* * * * *

专利名称(译)	OLED像素驱动电路和像素驱动方法		
公开(公告)号	US20180301091A1	公开(公告)日	2018-10-18
申请号	US15/519840	申请日	2017-03-16
[标]申请(专利权)人(译)	深圳市华星光电技术有限公司		
申请(专利权)人(译)	深圳市中国星光电科技有限公司.		
当前申请(专利权)人(译)	深圳市中国星光电科技有限公司.		
[标]发明人	KUANG JIMU WEN YICHIEEN		
发明人	KUANG, JIMU WEN, YICHIEEN		
IPC分类号	G09G3/3258		
CPC分类号	G09G3/3258 G09G2320/0646 G09G2300/0819 G09G2320/045 G09G2320/0233 G09G3/3208 G09G3/3233 G09G2300/0842 G09G2310/08		
优先权	201710104789.9 2017-02-24 CN		
其他公开文献	US10319304		
外部链接	Espacenet USPTO		

摘要(译)

本发明提供一种OLED像素驱动电路和像素驱动方法。OLED像素驱动电路利用7T2C结构，并包括第一N型薄膜晶体管(T1)，第二N型薄膜晶体管(T2)，第三N型薄膜晶体管(T3)，第四N型薄膜晶体管(Tb)，第五P型薄膜晶体管(T5)，第六N型薄膜晶体管(Tb)，第一电容器(C1)，第二电容器(C2)和有机发光二极管(D1)和第一扫描信号(Scan1)，第二扫描信号(Scan2)，第三扫描信号(Scan3)，发光控制信号(EM)和数据信号(Data)彼此组合以一个接一个地对应于复位级，阈值电压检测级，编程级和发光级。

